

not disclose a cache memory being directly coupled to the first host processor.

Applicants respectfully disagree with the Examiner's suggestion and submit that there is sufficient disclosure in the application as filed to support claim 37 as added in the May 9, 2002 Amendment. For example, on page 14, lines 7-17 a data cache 108, a VLW processor 102 and fixed function unit 106 are described all of which correspond respectively to "a cache memory," "said first host processor" and "said second local processor," as defined in claim 37. It is clear from Fig. 1A that the cache memory, which corresponds to data cache 108 and instruction cache 110, is directly connected with the first host processor (CPU CO 102 and CPU C1 104).

Accordingly, Applicants respectfully submit that the invention as defined in claim 37 contains subject matter which was adequately described in such a way as to be reasonably convey to person skilled in the art at the time the application was filed, and that the claimed subject matter was in the possession of the Applicants as of the date the application was originally filed.

In paragraph 3 of the Final Office Action, the Examiner has rejected claims 19-36 under 35 U.S.C. § 103 as being unpatentable over Reader et al. (U.S. Patent No. 6,192,073) in view of Kusters (U.S. Patent No. 5,819,112). The Examiner contends that Reader teaches all of the elements of the present invention except for a multiplexer coupled to the interface for providing access between a selected number of I/O device driver units to external I/O devices via output pins. However, the Examiner contends that Kusters teaches such an element and that it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the multimedia processor of Reader with the multiplexer of Kusters to arrive at the present invention as claimed.

In paragraph 10 of the Office Action, the Examiner has alternatively rejected claims 19-36 under 35 U.S.C. § 103 as being unpatentable over Reader et al. (U.S. Patent No. 6,192,073) in view of Kim (U.S. Patent No. 5,926,187).

In paragraph 13 of the Office Action, the Examiner has provisionally rejected claims 19-36 under the judicially created doctrine of obviousness type double patenting as being unpatentable over claims 1-18 of co-pending U.S. Patent Application No. 09/172,286 now U.S. Patent No 6,347,344.

Applicants respectfully disagree with the Examiner's contentions and submit the following remarks in response.

The present invention as claimed in claim 19, is directed to an integrated multimedia system having a multimedia processor disposed in an integrated circuit, wherein the multimedia system comprises a first host processor system coupled to the multimedia processor. A second local processor is disposed within the multimedia processor for controlling the operation of the multimedia processor. A data transfer switch is disposed within the multimedia processor and coupled to the second processor for transferring data to various modules of the multimedia processor. A data streamer is coupled to the data transfer switch, and configured to schedule simultaneous data transfers among a plurality of modules disposed within the multimedia processor, at least one of which is a cache memory, in accordance with corresponding channel allocations.

An interface unit is coupled to the data streamer having a plurality of input/output (I/O) device driver units. A multiplexer is coupled to the interface unit for providing access between a selected number of I/O device driver units to external I/O devices via output pins and a plurality

of external I/O devices are coupled to the multimedia processor.

In this configuration, the present invention is directed to reducing bandwidth delays by employing a data transfer arrangement that overcomes the disadvantages of the prior art utilizing a data streamer and interface unit which allow the data transfer switch to transfer information to a number of external I/O devices simultaneously. To this extent, the present invention features a cache memory, employed as a data transfer object of the data streamer. With this feature, the data streamer of the present invention transfers data among a plurality of modules, including the cache memory, significantly reducing cache misses, thus attaining continuous high-volume data transfer. As such, the data cache is a physical memory within the system that can be addressed by the data streamer, for example, by use of a DMA controller.

The cited prior art, namely Reader, teaches a method and apparatus for processing video data using three processors capable to operate concurrently, a scaler processor, a vector processor and a bit stream processor. In particular, as illustrated in columns 4 and 5 of the Reader reference, bitstream processor 245 does not include a data cache as a data transfer object.

Furthermore, as discussed in column 4, line 64 to column 5, line 1 of the Reader reference,

“These operations are suitable for a vector processor because these operations frequently need the same instruction to be performed on multiple pieces of data. Bitstream processor 245 performs Huffman decoding and encoding and zig-zag bitstream processing.”

Thus, as described, the bit stream processor of Reader is a Huffman encoding and decoding device which acts to processes data, rather than a data streamer for performing DMA transfer among a plurality of modules, including the cache memory, as disclosed in the present invention.

The cited prior art, namely Kusters, teaches an apparatus for controlling an I/O port by

queuing requests and in response to a predefined condition, enabling the I/O port to receive the interrupt requests. The Kusters reference provides a system and method for controlling parallel port peer to peer communication in personal computers.

The cited prior art, namely Kim, teaches video interface and overlay system and process. The Kim reference is directed to overcoming drawbacks in the prior art associated with inserting multiple video images into multiple video windows in the graphics images by providing a system for enhanced matching of video windows with video signals or video pixel maps.

Contrary to the Examiner's contentions, there is no teaching or suggestion in any of the cited prior art which discloses the present invention as claimed. For example, there is no teaching or suggestion in the cited prior art, either alone or in combination which teaches a data streamer coupled to the data transfer switch, and configured to schedule simultaneous data transfers among a plurality of modules disposed within the multimedia processor, at least one of which is the data cache, in accordance with corresponding channel allocations.

Therefore, Applicants respectfully submit that none of the cited prior art references, either alone or in combination, teach or suggest the present invention as claimed. As such, Applicants respectfully request that the rejection under 35 U.S.C. § 103 of independent claims 19 and 28 and claims 20-27 and 29-37 which depend therefrom be withdrawn.

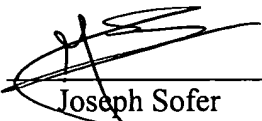
Applicants note that they will respond to the issue of double patenting with a Terminal Disclaimer after all other rejections have been removed.

In view of the aforementioned amendment and remarks, it is respectfully submitted that all claims currently pending in the above identified application are now in condition for allowance, the earliest possible notice of which is earnestly solicited. If in the Examiner's

opinion the prosecution of the present application would be advanced by a telephone interview,  
he is invited to contact the undersigned at the telephone number listed below.

Respectfully submitted,

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